REMARKS

Summary Of Office Action

Claims 1-41 and 43-53 are pending in this application.

Claims 1, 9, 11, 12, 25, 38, 41, 43, and 51-53 are objected to as containing various informalities.

Claims 1-3, 9, 13-15, 21, 25, 26, 29, 31, 32, 38, 43-45 and 51 are rejected under 35 U.S.C. § 103(a) as being obvious from Stevens et al. U.S. Patent No. 6,226,729 (hereinafter "Stevens") in view of Ikeda U.S. Patent No. 6,487,086 (hereinafter "Ikeda") in further view of Hartwell U.S. Patent No. 6,724,850 (hereinafter "Hartwell").

Claims 4, 5, 7, 8, 10-12, 16, 17, 19, 20, 22-24, 27, 28, 30, 33, 34, 36, 37, 39-41, 46, 47, 49, 50, 52 and 53 are rejected under 35 U.S.C. § 103(a) as being obvious from Stevens, Ikeda, and Hartwell in further view of Johnson et al. U.S. Patent No. 5,577,236 (hereinafter "Johnson").

Claims 6, 18, 35, and 48 are rejected under 35 U.S.C. § 103(a) as being obvious from Stevens, Ikeda, and Hartwell in further view of Olarig et al. U.S. Patent No. 6,134,638 (hereinafter "Olarig").

Summary of Telephonic Interview

Applicant and applicant's representative, Michael J. Chasan (Reg. No. 54,026), wish to thank the Examiner for the courtesy of the October 23, 2007 telephonic interview. During the interview, the Examiner and applicant's representative discussed the differences between the claimed invention and the cited references. During the interview, the Examiner agreed to reconsider the pending rejection in view of the following remarks.

Summary Of Applicant's Reply

Applicant has amended claims 1, 9, 11-13, 21, 23-26, 29-31, 38, 40, 41, 43, and 51-53 to more particularly define the invention. No new matter has been added and all of the amendments are fully supported by the original specification.

Reconsideration of this application in view of the amendments and the following remarks is respectfully requested.

Applicant's Reply to the Objections to the Claims

Claims 1, 9, 11, 12, 25, 38, 41, 43, and 51-53 are objected to as containing various informalities. Applicant's amendments to the claims have corrected these various informalities. Accordingly, applicant respectfully requests that these objections be withdrawn.

Applicant's Reply to the 35 U.S.C. § 103(a) Rejections

I. Rejection of Independent Claims 1, 9, 13, 21, 25, 26, 29, 31, 38, 43, and 51

Independent claims 1, 9, 13, 21, 25, 26, 29, 31, 38, 43, and 51 are rejected under 35 U.S.C. § 103(a) as being obvious from Stevens, Ikeda, and Hartwell.

Amended independent claims 11, 9, 13, 21, 25, 26, 29, 31, 38, 43, and 51 are, at least in part, directed toward methods, memory controllers, and apparatus for selecting an operating speed of a memory module interface. The number of memory modules is counted and a running tally of the number of memory modules is maintained based on the counting. Multiple clock signals are simultaneously generated at different frequencies to provide a selectable operating speed for the memory module interface. The maximum speed at which all of the memory module can operate is determined. A look-up table

containing a plurality of memory clock frequencies each associated with a number and a type of memory modules is accessed. Based on comparing a final tally of the number of memory modules with the look-up table, only one of the multiple clock signals is selected to provide the operating speed of the memory module interface, where the operating speed is slower than the determined maximum speed. The selected clock signal is then provided to all of the memory modules.

The Examiner's position in this rejection appears to be that (1) Stevens shows all of the features all applicant's independent claims except, (a) selecting an operating speed to be slower than the determined maximum speed and (b) simultaneously generating multiple clock signals at different frequencies, (2) Ikeda compensates for the first deficiency in Stevens by selecting an operating speed to be slower than the determined maximum speed based on a final tally of the number of memory modules, and (3) Hartwell compensates for the second deficiency in Stevens by simultaneously generating multiple clock signals at different frequencies. Applicant respectfully disagrees with the Examiner's position.

A. The Combination Of References Do Not Show Or Suggest All Of The Elements Of Applicant's Amended Independent Claims

None of these references, taken alone or in combination, show or suggest "accessing a look-up table containing a plurality of memory clock frequencies each associated with a number and a type of memory modules" and selecting a clock signal "based on at least comparing a final tally of the number of said memory modules with the look-up table," as recited by applicant's amended independent claims. Thus, applicant respectfully submits that neither Stevens nor Ikeda nor Hartwell shows or suggests all of the elements of

applicant's independent claims. Whether or not the combination of these references are proper, the combination of features which these references cumulatively contribute also falls short of showing or suggesting applicant's claimed

B. Stevens Does Not Show Or Suggest Selecting A Clock Signal Based On A Final Tally Of The Number Of Memory Modules

The Examiner contends that Stevens shows that a clock frequency is "selected based on a final tally of every memory modules that are operable with frequency – i.e., selected frequency is to be operable with final tally of memory modules." Applicant respectfully submits that Stevens does not show or suggest this feature.

Stevens refers to a method for configuring or initializing a memory device. During configuration or initialization, a clock generator is started in the memory controller. The frequency of the single generated clock signal is selected by "determining a channel frequency at which all [memory modules] may operate" (Stevens, column 13, lines 43-45). This determination is performed based on querying the SPD data of every RIMM module. The SPD data includes timing information (e.g., maximum frequency) for each device. Thus, Stevens only selects a single clock frequency based on the speed of the memory modules and not based on a final tally of the number of memory modules. Even though Stevens refers to maintaining a count of the number memory modules, there is nothing in Stevens that shows or suggests that this number is used to select a frequency at which the memory controller will operate. Thus, despite the Examiner's contention, this element is not shown by Stevens. Therefore, Stevens does not show selecting a frequency "based on at least comparing a final tally of the number of said memory modules

with the look-up table" as recited by applicants' amended independent claims. Furthermore, neither Ikeda nor Hartwell make up for this deficiency in Stevens.

C. Ikeda Does Not Show Or Suggest A Method For Selecting An Operating Speed of A Memory Module

The Examiner contends that Ikeda shows "a method for selecting an operating speed of a memory module interface [wherein] although the memory modules can operate at maximum speeds greater than 133 MHz, the slower 100 MHz based on a final tally of 4 memory modules is provided as the operating speed to avoid reflections and distortions." Applicant respectfully submits that Ikeda does not show or suggest this feature.

In the "Background of the Invention," Ikeda mentions that in some systems the number of memory modules that can be connected to parallel memory sockets may be limited by the frequency of the memory control clock. For example, when the control clock frequency is 100 MHz only four memory modules may be connected and when the control clock frequency is 133 MHz only two memory modules may be connected. See, Ikeda, column 1, lines 45-62. Ikeda refers to improved contact terminals for memory modules that reduce this problem by improving the impedance matching between the main board and the memory modules. However, Ikeda does not show or suggest a method for selecting an operating speed of a memory controller based on the number of memory modules. Rather, Ikeda merely refers to improving impedance matching in contact terminals in order to permit the use of high frequency clock signals with multiple memory modules. In fact, instead of adjusting the clock frequencies based on the number of memory modules, Ikeda suggests that in prior art systems a clock speed was selected and that the number of memory modules that can be connected would be determined based on this number. Applicant's claimed

approach for selecting an operating speed in response to comparing a final tally of the number of memory modules with the look-up table patentably improves on this approach. Therefore, Ikeda does not show selecting a frequency "based on at least comparing a final tally of the number of said memory modules with the look-up table" as recited by applicants' amended independent claims. Furthermore, neither Stevens nor Hartwell make up for this deficiency in Ikeda.

D. Conclusion

For at least this reasons applicant respectfully requests that the rejection of independent claims 1, 9, 13, 21, 25, 26, 29, 31, 38, 43, and 51 under 35 U.S.C. § 103(a) as being obvious from Stevens, Ikeda, and Hartwell be withdrawn.

II. Rejection of Independent Claims 11, 12, 23, 24, 30, 40, 41, 52, and 53

Independent claims 11, 12, 23, 24, 30, 40, 41, 52, and 53 are rejected under 35 U.S.C. § 103(a) as being obvious from Stevens, Ikeda, and Hartwell in further view of Johnson.

Applicant respectfully submits that amended independent claims 11, 12, 23, 24, 30, 40, 41, 52, and 53 are allowable for at least the same reasons as amended independent claims 1, 9, 13, 21, 25, 26, 29, 31, 38, 43, and 51. Thus, neither Stevens nor Ikeda nor Hartwell nor Johnson shows or suggests all of the elements of applicant's amended independent claims. Whether or not the combination of these references are proper, the combination of features which these references cumulatively contribute also falls short of showing or suggesting applicant's claims. For at least this reasons applicant respectfully requests that the rejection of independent claims 11, 12, 23, 24, 30, 40, 41, 52, and 53 under 35 U.S.C. § 103(a) as being obvious from Stevens, Ikeda, Hartwell, and Johnson be withdrawn.

II. Rejection of Dependent Claims

For at least the reasons discussed above with respect to applicant's amended independent claims, dependent claims 2-8, 10, 14-20, 22, 27, 28, 32-37, 39, and 44-50, which depend directly or indirectly from claims 1, 9, 11-13, 21, 23-26, 29-31, 38, 40, 41, 43, and 51-53 are also not rendered obvious from the various combinations of Stevens, Ikeda, Hartwell, Johnson, and Olarig (i.e., dependent claims are patentable if their independent claim is patentable). Accordingly, applicant respectfully requests that the rejections of dependent claims 2-8, 10, 14-20, 22, 27, 28, 32-37, 39, and 44-50 be withdrawn.

Conclusion

The foregoing demonstrates that claims 1-41 and 43-53 are patentable. This application is therefore in condition for allowance. Reconsideration and allowance are accordingly respectfully requested.

Respectfully submitted,

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